

#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/500,657
 Applicant : Josef BERWANGER et al.
 Filed : February 14, 2005
 TC/A.U. : Unknown
 Examiner : Unknown

Docket No. : (04:81)
 Customer No. : 02119

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Date: February 14, 2005

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97(b),
 AND EXPLANATION OF THE RELEVANCE OF THE CITED PRIOR ART**

Sir:

The undersigned hereby requests that the prior art cited on the attached prior art statement be placed of record in the application file and be considered by the examiner.

This citation of prior art is made under 37 CFR 1.97(b), since it is being filed before the mailing date of a first Office action.

The relevance of the prior art cited on the attached form 1449 is as follows:

6,011,801

According to the teachings of this patent, information flow in the form of individual channels of digital data across a time division multiplex (TDM) bus is controlled when the bandwidth b_c of an individual channel may not be integrally related to the bandwidth b_t of individual time slots of the TDM bus. A channel is assigned to a selected number m of TDM bus time slots, where $m=n$ and the relationship between b_c and b_t is given by the expression $(n-1)b_t < b_c \leq nb_t$. Sequential bytes of data from the channel are transmitted during data byte opportunities in the channel's selected time slots. A validity identification signal is generated for each data byte transfer opportunity in the selected time slots, and a predetermined binary state is transmitted substantially simultaneously with each data byte transfer opportunity. A VALID signal is transmitted, independently of the TDM bus, substantially simultaneously with each data byte transfer opportunity filled by the channel. To permit selected bandwidth in the reverse direction to be controlled over a bidirectional TDM bus, a separate bandwidth request signal may also be transmitted, substantially simultaneously with data byte transfer opportunities in the forward direction but also independently of the TDM bus.

6,138,200

This patent teaches a system and method for arbitrating amongst a plurality of applications requesting bus access. Based on the applications requesting bus access, a bus frame is calculated, and a plurality of bus duration time slots within the bus frame are determined. For each bus duration time slot, a priority is assigned to each application requesting bus control and a bus allocation table is created. A bus master controller then

allocates control during each bus duration time slot in accordance with the priorities in the bus allocation table.

WO 99/55036

This publication teaches methods and apparatuses for allocating time slots to circuit-switched channels established to comprise one or more respective time slots in a recurrent frame of a time division multiplexed network. According to the invention, a time slot allocated to said channel is associated with a selected level, of at least two available levels of priority. Decisions as to whether or not to deallocate said time slot from said channel is then based upon a comparison of said selected level of priority and a level of priority associated with a request for a time slot for another channel.

WO 93/25017

This publication teaches a method for transferring ancillary information, such as channel-associated signaling and alarms in a basic time-division multiplex system, where ancillary information is transferred in a predetermined time slot (TS16) of each frame, and where information associated with more than one channel is transferred in at least one time slot (TS1...TS15, TS17...TS31) of the basic system. To provide a method allowing the ancillary information, particularly signalling and alarms, to be transferred with as high compatibility as possible in a conventional basic multiplex system up to a capacity of 120 speech channels, a superframe (12) having the length of several multi-frames (11) is assembled, and at least part of the ancillary information is transferred in said predetermined time slot (TA16) so that the number of the multi-frame is transmitted in addition to said

ancillary information, the number indicating with which channel the ancillary information is associated.

WO 98/00941

According to the teachings of this publication, in a subscriber loop equipment (10) having a subscriber bus (26), there is provided an odd data stream carrying a first set of data time slots of an E1 signal and a first set of signaling and control time slots of the E1 signal. Also provided is an even data stream carrying a second set of data time slots of the E1 signal and a second set of signaling and control time slots of the E1 signal. The odd and even data streams are bit-interleaved and transported on the subscriber bus (26).

DE 197 06 081 A1

This patent teaches a method involving transmitting data bits in a sequence of time frames (202, 204, 206). The number of bits in each time frame corresponds to the Integrated Services Digital Network (ISDN) standard. At least one useful channel uses packet-orientated transmission, and the transmitted assembled data packet includes a packet identifier. The complete frame which is transmitted in 1.5 ms, contains 26 useful channels, each having time slots allotted for 8 bits. The data in each channel are collected into packets, with the packet identifier (221) in bit position 18, following a packet identifier (220) for the complete frame in position 17 of the first sub frame (202). The packet identifier (221) has at least one fixed adjustable position in at least one time frame of the sequence of transmitted time frames. Preferably the packet identifier has a fixed predetermined position within the ISDN standard predetermined service frame.


Appl. No. 10/500,657
IDS filed February 14, 2005
Prior to first Office action

**K. Etschberger et al., Buscontrollerbaustein für echtzeitfähige Netze, Electronik 25,
August 12, 1989, Pages 79-83**

There is no translation available for this publication. It is being cited to show the state
of the art.

Examination of this application is respectfully requested.

Respectfully submitted,


Ronald E. Greigg
Registration No. 31,517
Attorney for Applicants
Ref. #20893

GREIGG & GREIGG, PLLC
1423 Powhatan Street, Suite One
Alexandria, VA 22314

Telephone: 703-838-5500
Facsimile: 703-838-5554

REG/elb
Customer No. 02119

J:\Dreiss, Fuhlendorf\10500657\05-02-11, 0481, IDS under 1.97(b).wpd

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

(04:81)

Application Number

10/500,657

Applicant(s)

Josef BERWANGER et al.

Filing Date

02-14-2005

Group Art Unit

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,011,801	01-04-2000	SOLOMON			
		6,138,200	10-24-2000	OGILVIE			

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
		WO 99/55036	10-28-1999	PCT			✓	
		WO 93/25017	12-09-1993	PCT			✓	
		WO 98/00941	01-08-1998	PCT			✓	
		DE 197 06 081 A1	08-20-1998	Germany				✓

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		K. Etschberger et al., Buscontrollerbaustein für echtzeitfähige Netze, Electronik 25, August 12, 1989, Pages 79-83

EXAMINER	DATE CONSIDERED
----------	-----------------

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.